REMARKS

Claims 1-3 and 5-19 are all the claims presently being examined in this application. Claim 1 has been amended to more particularly define the claimed invention. Claim 4 has been canceled. Claims 5-19 have been added to claim additional features of the claimed invention.

It is noted that the amendments are made only to more particularly define the invention and **not** for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1 and 3 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Gelke et al. (U.S. Patent No. 6,735,661).

Claims 2 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Muramatsu et al. (U.S. Pat. No. 6,384,832) in view of Gelke et al.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as defined, for example, by independent claim 1) is directed to a memory device including a data memory to and from which data is input and output via a data bus for the data memory. A plurality of buffer circuits inputs and outputs image data to and from the data memory via a first data bus that has a bus width equal to that of the data bus for the data memory and is electrically connected to the data bus for said data memory.

Additionally, image data is input and output to and from a data processing circuit via a second data bus having a bus width smaller than the data bus for the data memory. An arbitration circuit is connected between the data processing circuit and the a plurality of buffer circuits and controls the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period. (See the Specification at page 4, line 20 to page 5, line 10.)

Conventionally, in order to shorten write time for writing data to a memory and read-out time for reading data out of the memory, the bus width of the data bus connected to the memory is enlarged. Enlarging the bus width, however, may result in more complicated wiring. (Specification at page 1, lines 8-12).

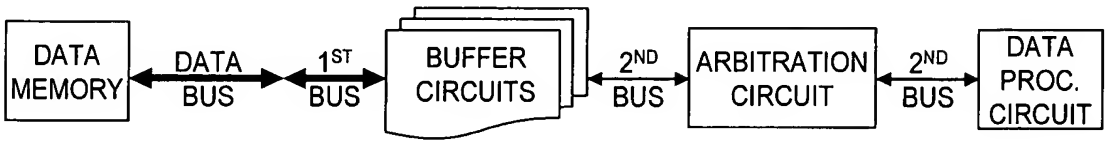
The claimed invention (e.g., as recited in claim 1), on the other hand, includes an arbitration circuit, connected between a data processing circuit and a plurality of buffer circuits, for controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period. Thus, image data processing of different images can be executed simultaneously. (Specification at page 3, lines 9-17.)

II. THE ALLEGED PRIOR ART REJECTION

The Examiner alleges that Gelke et al. teaches the claimed invention of claims 1 and 3, and that Muramatsu et al. in view of Gelke et al. teaches the claimed invention of 2 and 4. Applicant has amended independent claim 1 with the subject matter of dependent claim 4. Therefore, the following arguments for independent claim 1 are with respect to the alleged rejection over Muramatsu et al. (Muramatsu) in view of Gelke et al. (Gelke). Applicant submits, however, that Muramatsu and Gelke, neither alone nor in combination, teach or

suggest each every element and feature of the claimed invention.

For purposes of clarity, Applicant characterizes each of the elements of independent claim 1 as follows:



a data memory to and from which data is input and output via a data bus for the data memory;

a plurality of buffer circuits for inputting and outputting image data to and from said data memory via a first data bus that has a bus width the same as that of the data bus for said data memory (characterized by the equivalent bolding of the data bus and the 1st bus) *and that is electrically connected to the data bus for said data memory, and inputting and outputting image data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory* (characterized by the thin width of the 2nd bus with respect to the bolded data/1st bus widths)*; and*

an arbitration circuit, which is connected between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period.

The Office Action equates Applicant's *arbitration circuit* and *buffer circuits* to Muramatsu's data transfer part 20 and data holding parts A-F, respectively, of the data control unit 4 of Fig. 6.

However, in contrast to Applicant's claim language reciting the, "*...arbitration circuit, ... is connected between the data processing circuit and said plurality of buffer*

circuits," Muramatsu fails to teach the data transfer part 20 connected **between** the data holding parts A-F and a data processing circuit.

Furthermore, the Office Action failed to state what element of Muramatsu allegedly teaches or suggests Applicant's *data processing circuit*. Applicant assuming *arguendo* that an equivalent element in Muramatsu could be the function control unit 50, or image processing units 80 or 90, of Fig. 3, since they all communicate with data control unit 4 wherein the data transfer part 20 resides.

However, image processing units 80 and 90 of Muramatsu, assuming *arguendo* to be equivalent with Applicant's *data processing unit*, are directly connected to the data holding parts A-F, and not to the data transfer part 20, thereby failing to teach or suggest an "*...arbitration circuit, ...connected between the data processing circuit and said plurality of buffer circuits*."

Additionally, function control unit 50 of Muramatsu, again, assuming *arguendo* to be equivalent with Applicant's *data processing unit*, merely controls each function of the image processing units 80 and 90 by sending control signals from CPU 1, (column 5, lines 38-40, and column 6, lines 62-66). There is no teaching or suggestion in Muramatsu *that image data is input and output to and from* the function control unit 50. The only purpose of the function control unit 50 is to send control signals to control the image processing units 80 and 90.

Therefore, Muramatsu fails to teach or suggest, "*inputting and outputting image data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory*," and "*an arbitration circuit, which is connected between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits.*"

With respect to the rejection of Applicant's claims, Applicant respectfully submits

that Muramatsu would not have been combined with Gelke and even if combined, the combination would not teach or suggest each and every element of the claimed invention, since Muramatsu, as pointed out above, fails to teach or suggest each and every element of the claimed invention, and Gelke, as stated by the Examiner to lack Applicant's claimed arbitration circuit, fails to overcome the deficiencies of Muramatsu.

Specifically, Gelke fails to teach or suggest "*an arbitration circuit, which is connected between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period.*" Therefore, the Examiner is respectfully requested reconsider and withdraw this rejection.

Therefore, none of the cited prior art references nor any alleged combination thereof teach or suggest each and every element of Applicant's claimed invention. Applicant respectfully requests that the Examiner reconsider and withdraw the rejections.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3 and 5-19, the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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